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Design of High Performance of 2×4 Decoder Using 16 nm Technology.

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ABSTRACT

This study is an analysis of the Modified Mixed Logic Design (MMLD). It is a hybrid of three different types of logic: CMOS, Dual-Value Logic (DVL), and the Gate Diffusion Input (GDI) mechanism. We want to reduce power consumption and delay time by comparing two decoder systems, one utilising 14 transistors and the other using 15. Along with conventional decoders, all of them use inverted ones. By providing full voltage swing with a significantly reduced transistor count (about 12), the proposed decoders save time and power when compared to conventional CMOS logic, according to the study. In SPICE simulations conducted at the 16nm technology node, the proposed 12-transistor 2x4 decoder outperformed traditional logic designs.

Keywords: CMOS, Dual-Value Logic (DVL), Gate Diffusion Input (GDI) and 2x4 decoder.

INTRODUCTION

Static CMOS circuits are the building blocks of most integrated circuit logic gates. The pMOS pull-up network and the nMOS pull-down network include CMOS (Complementary Metal-Oxide-Semiconductor) circuits, which have beneficial performance characteristics such as noise and device fluctuation resistance. In addition to being able to rely on small transistors even at low voltages, CMOS circuitry has additional advantages. The fact that inputs are provided only to the gate terminals of transistors in complementary metal-oxide-semiconductor (CMOS) circuits limits their use to cell-based logic design and synthesis, which is a significant limitation. Developed in the 1990s as a replacement for complementary metal-oxide-semiconductor (CMOS) logic, pass transistor logic (PTL) reduced space requirements, improved power efficiency, and increased processing speed. In pass transistor circuits, the key difference is that inputs may be connected to the

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source/drain diffusion terminals or the gate of the transistor, rather than only the gate. Either individual pMOS or nMOS transistors, or a transmission gate constructed by connecting the two kinds of transistors in parallel, may be used to design a pass transistor circuit. The rapid advancements in VLSI (Very Large Scale Integration) technology, such as miniaturisation and voltage scaling, have heightened the need for logic devices that are efficient in terms of power consumption, processing speed, and total space utilisation. Particularly urgent is the need for low-power design in high-performance computer systems, such as digital signal processors and microprocessors. Fundamental to these setups is the decoder, a combinational circuit that receives a code as input and produces a stream of signals as output. Many diverse settings make use of line decoders. Some examples include data demultiplexing, seven-segment displays, address decoding in memory arrays, and microchip or microcontroller based frameworks.

Static random access memory (SRAM) systems rely heavily on the decoder's architecture, which impacts the SRAM block's power consumption and access time. This paper introduces a novel mixed-logic method for building decoders with low latency, transistor count, power consumption, and power consumption. Modern integrated circuits, and SRAM-based systems in particular, place a premium on minimal power usage and optimal space utilisation throughout design. Decoders are essential to memory address decoding since they are responsible for activating certain memory cells based on the addresses provided. When designing these decoders, keep in mind that the overall power consumption, speed, and footprint of the SRAM system are all impacted. In order to maintain system performance while meeting severe energy restrictions, it is becoming more important to achieve designs that are both low-power and area-efficient. This is shown in the 16nm process.This research proposes a fresh layout for a 2×4 decoder targeted at SRAM applications, using the 16nm CMOS technology node. While decreasing the amount of transistors, the design prioritises speed and reliability using state-of-the-art low-power techniques.

2.LITERATURE SURVEY

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2.1 Design of Low Power, High-Performance 2-to-4 and 4-to-16 Mixed-Logic Line Decoders

The consistency, resistance to noise, and device variation tolerance of static CMOS logic make it an ideal choice for integration into logic gates. The complementary nMOS pull-down and pMOS pull-up networks allow CMOS devices to function successfully with lower voltages and fewer transistors. Its scalability allows low-voltage operation with minimum design complexity, which is a major benefit of complementary metal-oxide semiconductors (CMOS). Complicating cell-based synthesis and limiting design flexibility, static CMOS only applies inputs to the gates of transistors.

Developed in the 1990s as a replacement for conventional complementary metal-oxide-semiconductor (CMOS) logic, pass-transistor logic (PTL) significantly reduced power consumption, wasted space, and processing times. In contrast to CMOS circuits, PTL circuits allow you to connect inputs to the source and drain terminals of a transistor gate. Using a pass-transistor circuit with a single nMOS or pMOS transistor is one possibility; using transmission gates, which are combinations of the two types of transistors, in parallel is another. Because of its adaptability, PTL is a great material for creating small, high-performance circuits.

2.2 Logic circuits for low-power two-to-four and four-to-16 line decoding

The nMOS pull-down and pMOS pull-up networks of static CMOS logic provide excellent efficiency and noise resistance, which are extremely advantageous to modern very large scale integration (VLSI) technology. Complementary metal-oxide-semiconductor (CMOS) logic has a few benefits, including as small transistor sizes, efficient low-voltage operation, and easy voltage scaling. As technology nodes shrink in size, leakage currents and transistor variances are growing, despite Moore's Law's continual advances in transistor density and performance. A more efficient, faster, and smaller alternative to complementary metal-oxide semiconductors (CMOS), pass-transistor logic (PTL) arose in response to these demands. Transistors use PTL to apply inputs to their gates, source, and drain terminals. You may build a PTL circuit with a single nMOS or pMOS transistor, or

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you can employ transmission gates, which are collections of transistors.Among the many common uses for decoders in memory systems are address decoding, data multiplexing, and signal selection, among others. Memory access efficiency and power consumption in systems like SRAM (Static Random Access Memory) are determined by the appropriate functioning of these circuits.

2.3 Decoder Design Various Mixed Logic Use Cases

Technological advancements in very large scale integration (VLSI) have made it possible to pack an increasing amount of transistors onto a single chip, opening the door to the creation of sophisticated, high-speed systems. Choosing the right logic types for combinational circuits is critical for meeting the demand for low-power designs, as the design of decoders may significantly impact total power consumption. Capacitance of the switch, activity of the transition, and currents in short circuits are important variables that affect power dissipation. Power efficient decoders are vital for applications that need low power consumption, such memory systems, digital signal processing (DSP), and microprocessors. When it comes to SRAM systems, decoders are crucial for managing memory access. Decoder design has a significant impact on memory system performance and power consumption. For current systems to make advantage of SRAM as on-chip cache memory, efficient row and column decoders are crucial for reduced power consumption and quicker data access.

Dividers for Two to Four Mixed-Logic Lines in a Modular Design (1.4) Implementing a Chronological Approach

Digital signal processors, microprocessors, and mobile devices are examples of high-performance applications that place a heavy emphasis on low power design in modern very large scale integration (VLSI) systems. As chip density and clock rates continue to rise, the energy needs of small devices are on the rise, making low-power circuit design more important. Decoders are combinational circuits that can take binary input codes and generate a matching set of output signals. Data multiplexing, display systems, memory address decoding, and many other applications make extensive use of them.Numerous low-power decoder methods have been suggested to meet the

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increasing need for energy-efficient gadgets. One approach that uses a clock to regulate power usage is controlling the timing of signal transitions and selectively activating decoder circuitry. The low power consumption and rapid access times required by SRAM applications make these technologies particularly useful.

Building Relatively Small n-to-2n Code Breakers Chapter 2.5

Decoders are essential components of digital circuits that are used by address decoders and multiplexers. With millions of address lines to decode, designing efficient decoders is crucial for huge memory systems to reduce power consumption and increase speed. With hierarchical decoders or pre-decoding techniques, scaling decoder circuits becomes a breeze. One use of multiplexers and binary tree decoders is the construction of small decoders that exhibit exceptional speed performance while using very little power. Modularly incorporating AND gates and 1-to-2 decoders into n-to-2n decoder designs allows for the incorporation of bigger decoders. By breaking down decoders into smaller, more manageable components, their power consumption may be easily increased or decreased.

Efficiency in Power and Space for SRAM Line Decoders (2.6)

Since current computer devices rely heavily on memories like SRAM, power efficiency in memory systems is of the utmost significance. Given the substantial space needed by memory cells on the device, reducing power in this area might have a substantial effect on total power usage. Designers may drastically cut down on decoder circuit power consumption by using the right logic type. Switch capacitance, transition activity, and short circuit currents are important elements that impact power dissipation.When it comes to power consumption and access time, the designs of the decoders have a direct impact on SRAM systems, which are crucial to memory access management. Power efficiency and quick access times might be achieved by techniques such as improving decoder designs for certain combinations of SRAM and employing low-power logic types.

The 128x128 6T SRAM Row Decoder 2.7.1 Improvements

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For on-chip cache memory in particular, modern very large scale integration (VLSI) systems rely on quick, power-efficient SRAMs. There has been a performance bottleneck due to memory access times being slower than CPU speeds. Optimising SRAM architectures for scalability requires low-power solutions. The power consumption and access time of SRAMs are significantly impacted by address decoders. The effectiveness and speed of SRAM decoders have been the subject of much research and development. Two examples of such approaches are Wilson current mirror-based systems and hierarchical decoders with pre-decoding.

2.8 A Novel Approach to SRAM Decoder Architecture

Secure Random Access Memory (SRAM) is a popular choice for digital and computer systems due to its compatibility with processor speeds and fast access time. Processors depend on SRAM cache memory to be operational when the memory access latency keeps increasing. Because they control how quickly and efficiently memory cells may be accessed, address decoders are an essential part of SRAM memory blocks. Minimising memory access time and power consumption are two major implications of address decoder design. To maximise the efficiency of SRAM, several techniques are used, such as hierarchical decoders and pre-charging dynamic decoders.

2.9 Address Decoders with Excellent Performance and Minimal Power Consumption Address decoders for "Selective Precharge Memory systems" must be fast and efficient. Reducing power usage without sacrificing access times has been achieved via the creation of selective precharge technologies like AND-NOR and precharge decoders based on sensing amplifiers. Through selective line precharging, these techniques lessen wasteful switching and short-circuit currents. Consequently, they are more efficient and perform better than conventional decoders.

Compact, efficient, and dependable systems decoders may be developed using mixed-logic lines that have 2-to-4 and 4-to-16 inputs.

Recent developments in very large scale integration (VLSI) technology have opened the door for memory applications to use low-power, high-performance decoders. Decoders might be optimised for speed and power efficiency using mixed-

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logic design approaches such as hybrid CMOS and pass-transistor logic. Compared to conventional CMOS-based decoders, these methods provide significant benefits for SRAM applications prioritising speed and power efficiency. Memory system performance and power consumption may both be enhanced using mixed-logic designs, according to simulations.

3. EXISTING DESIGN

3.1 Design of Low Power, High Performance 2-4 and 4-16 Mixed-Logic Line Decoders

A 2-4 line decoder generates the four bare minimum terms, D0-3, from two input variables, A and B. Table I provides a synopsis of its logic functioning. Based on the input combinations, a value between 0 and 1 is assigned to each of the four outputs. Given that the inverted 2-4 decoder produces the complementary minterms I0-3, the selected output is set to 0 while the others are set to 1, as shown in Table II.

TABLE I
TRUTH TABLE OF 2-4 DECODER

A	B	D_0	D_1	D_2	D_3
0	0	**1**	0	0	0
0	1	0	**1**	0	0
1	0	0	0	**1**	0
1	1	0	0	0	**1**

TABLE II
TRUTH TABLE OF INV. 2-4 DECODER

A	B	I_0	I_1	I_2	I_3
0	0	**0**	1	1	1
0	1	1	**0**	1	1
1	0	1	1	**0**	1
1	1	1	1	1	**0**

The ability to accomplish logic operations with four transistors, rather than six, makes NAND and NOR gates the favoured choice in traditional complementary metal-oxide semiconductor (CMOS) architecture. A 2-4 decoder may be built using twenty transistors and two inverters and four NOR gates, as seen in Figure 1(a). A similar inversion

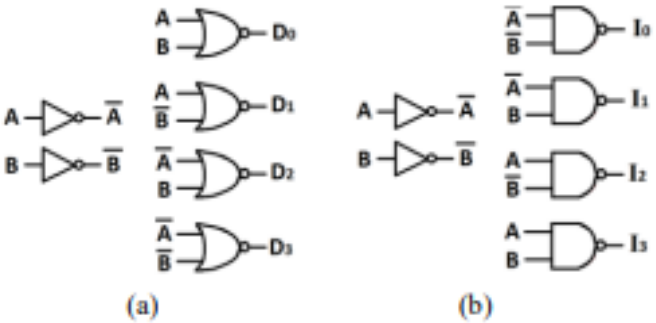

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Fig 3.1.1 : 20-Transistor 2-4 line decoders implemented with CMOS logic

Non inverting NOR-Based decoder (b) inverting NOR-Based decoder

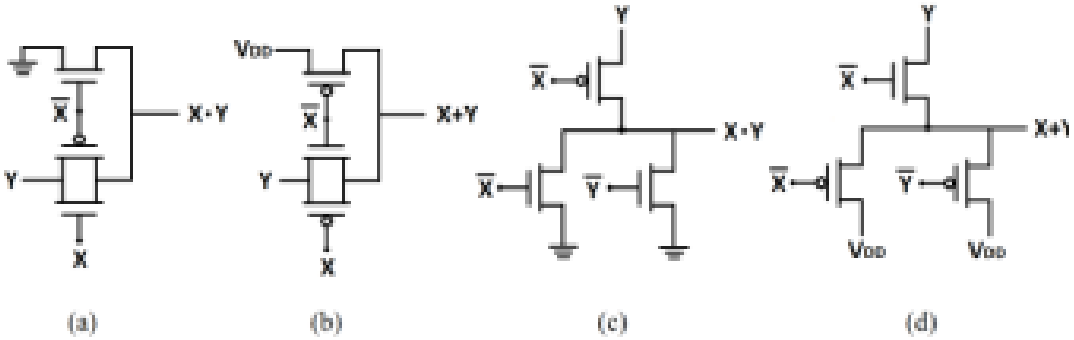

Fig 3.1.2 : 3-Transistor AND/OR gate considered in this work (a) TGL,AND gate

(b) TGL OR gate (c) DVL AND gate (d) DVL OR gate

Transmission gates have mostly been used in combinational logic as the primary switching component of multiplexers and XOR-based circuits, such as full adders. However, as shown in, we consider their potential use in developing AND/OR logic for use in line decoders. This is shown in Figure 3(a) and 3(b), respectively, by the two-input TGL AND/OR gates. Despite the fact that they are not fully swinging, they do restore for most input combinations. There are mainly two kinds of pass-transistor logic circuits: those that utilise nMOS pass-transistors alone (CPL) and those that employ both nMOS and pMOS. Here, we zero in on DVL as a method that outperforms DPL while reducing the amount of transistors needed to provide complete swing functionality. This picture shows the DVL AND/OR gates with two inputs.

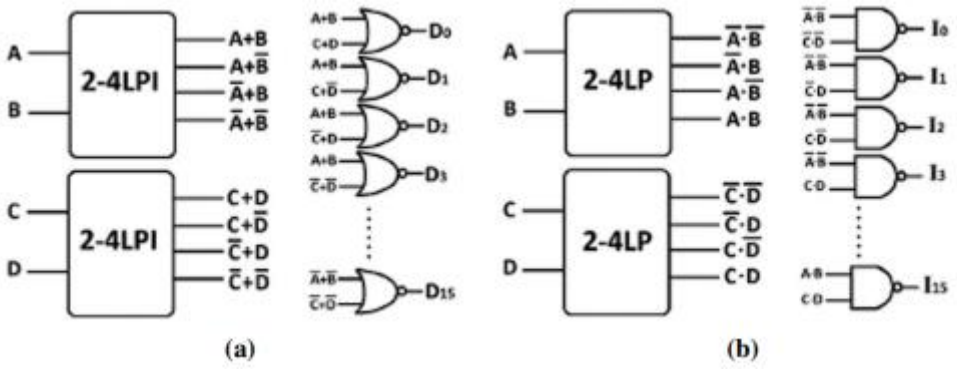

Fig 3.2: Decoding logic circuit using low power technique.

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4. PROPOSED METHOD WITH RESULTS

4. 1 schematic of line decoder based on 2-4 LPI

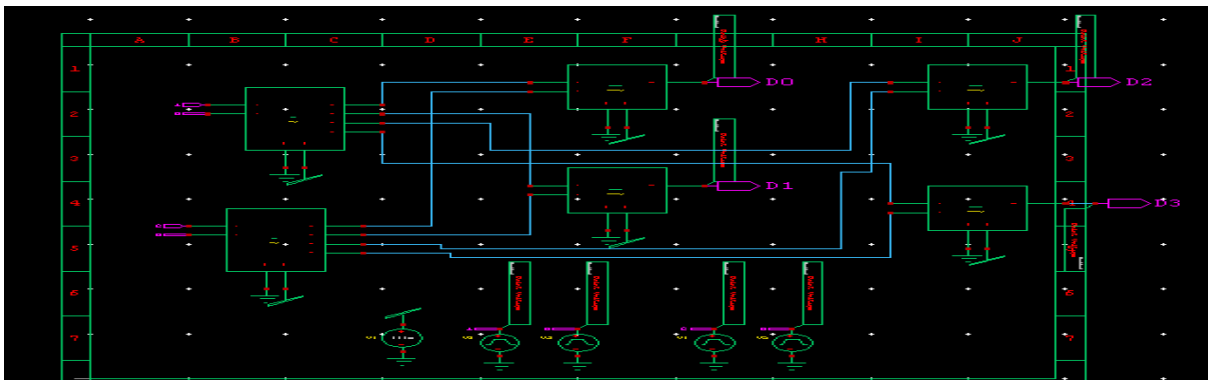

Fig.4.1. schematic of line decoders - based on 2-4 LPI

In the 2000s, pass transistor logic (PTL) was introduced as a low-power, high-speed, and small-area alternative to complementary metal-oxide-semiconductor (CMOS) logic. Figure 1 displays both the conversion gate logic (TGL) [2-8] and the dual-value logic (DVL) [2-8]. Two types of transistors, NMOS and PMOS, are used to build pass transistor circuits. In order to create a transmission gate (TG), two NMOS and PMOS devices are linked in tandem.

Here is the circuit in action, as seen in Figure 1. Five transistors and input buffers are needed for the design. It is common in PTL asymmetric architectures because, unlike CMOS logic, they are not balanced. Figures 2 and 3 show low power consumption with inverted outputs (LPI), high performance with inverted outputs (HPI), and low power consumption with high performance (LP), respectively, based on this circuit's variation from the one in figure 1 [11]. Table 1 shows that the circuits shown above demonstrate that a low power decoder design only needs fourteen transistors, in contrast to the fifteen transistors needed for a high performance decoder implementation. Table 1 displays the total number of PMOS and NMOS transistors used by CMOS and mixed logic decoders.

Using the matrix building approach, high-bitrate decoders are constructed. The four 4-16 decoders seen in Figures 2 and 3 are early CMOS NOR/NAND decoders.

In order to construct the circuits mentioned before, the SAED 14nm SPICE model

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libraries are used [9]. You can see the results of the simulation in the figure.

This short showcased the effective use of TGL, DVL, and static CMOS in the mixed-logic design of decoder circuits. Compared to traditional CMOS decoders, our four distinct 2-4 line decoder topologies—2-4LP, 2-4LPI, 2-4HP, and 2-4HPI—use fewer transistors while delivering better power delay performance. Additional line decoder topologies that were developed were the 4-16LP, 4-16LPI, 4-16HP, and 4-16HPI. These topologies were implemented by combining pre-decoding circuits from mixed-logic 2-4 decoders with static CMOS post-decoders. The suggested designs clearly outperformed the alternatives in the great majority of instances after a series of comparative spice simulations conducted at 32 nm. Space and power conservation should be your first priority, in which case the 2-4LP or 4-16LPI topologies are perfect. The 2-4LPI, 2-4HP, and 4-16HPI topologies, as well as their variations, the 4-16LP, 4-16HPI, and 4-16HP topologies, have all shown useful and efficient performance. Because of this, they may be used as foundational elements for more advanced combinational circuits, multiplexers, and decoders that meet different performance standards. Both bulk CMOS and surface-on-insulator (SOI) devices may benefit from the lower transistor count and low power properties that were described. The output circuits are implementable at the layout level and are compatible with RTL design and standard cell libraries.

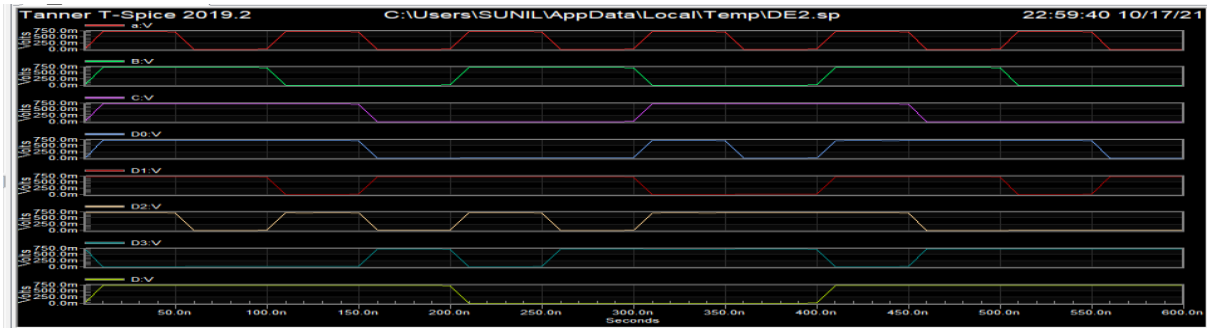

Fig.4.2. Simulation results of line decoders - based on 2-4 LPI

The results of the 2-4 LPI line decoder simulation are shown in the image up above.Last time, we covered 14-transistor low-power decoder topologies; in the worst-case situation, the delay is caused by the complementary propagation signal utilised in minimum terms D0 and I3.

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You may get around this restriction by making use of regular CMOS logic gates to generate these minimal terms; these gates don't need complementary inputs. A CMOS NOR gate is used to construct the minimum term D0, and a CMOS NAND gate is used to implement I3; an extra transistor is added to each structure. High Performance (HP) decoders are the result of this modification, which integrates three types of logic (CMOS, TGL, and DVL) into a single circuit to increase power and delay performance. The 2-4 HP and 2-4 HPI decoder schematics are shown in the image that follows.

4.2 schematic of line decoder based on 2-4 HPI

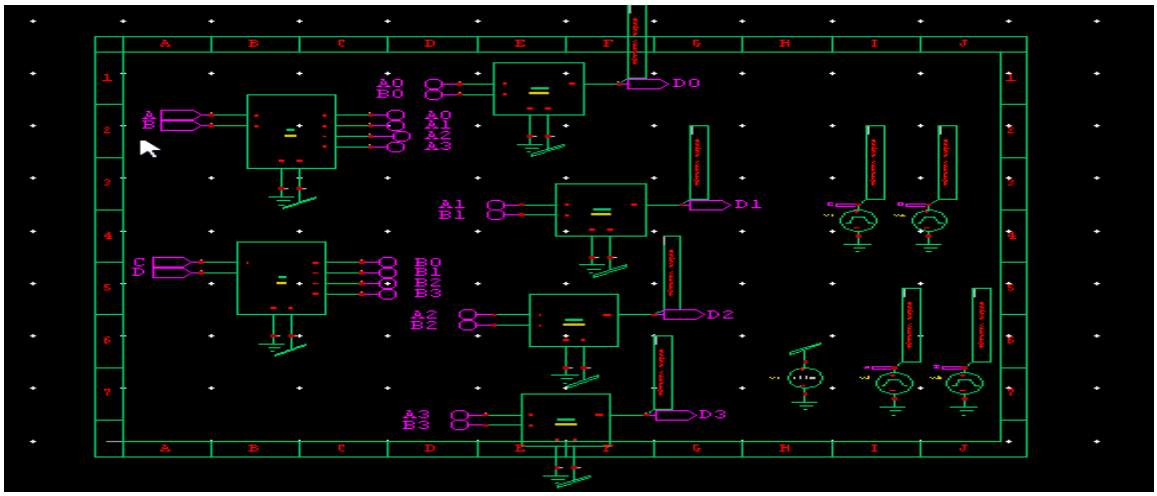

Fig.4.3. schematic of 2-4 HPI decoders

The worst-case latency is a drawback of the low-power topologies that were before discussed. This is due to the fact that the propagation signal is complementary A in the case of D0 and I3. When building D0 and I3 using static CMOS gates, complementary signals aren't needed. With complementary metal-oxide-semiconductor (CMOS) NOR gates and NAND gates, one more transistor may be added to the D0 topology and the I3 topology, respectively. The new 15T designs provide a significant reduction in latency with only a little increase in power dissipation. The designations "2-4HP" and "2-4HPI" indicate a 9 nMOS and 6 pMOS arrangement, respectively, and stand for "high performance" and "inverting," respectively. Figure 2 shows the 2-4HP and 2-4HPI schematics.

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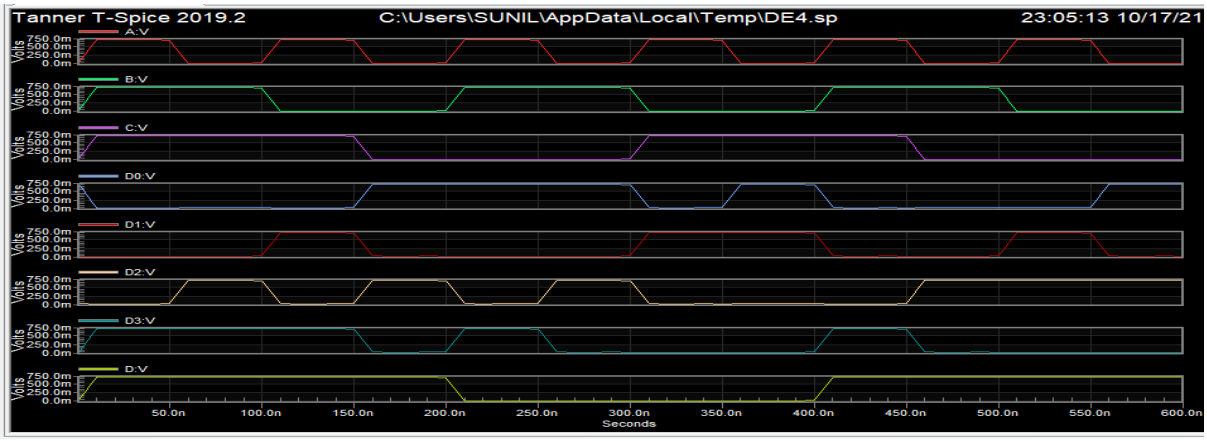

Fig.4.4. Simulation results of 2-4 HPI decoders

The picture up there shows the outcomes of a line decoder's simulation using 2-4 HPI. More efficient than complementary metal-oxide-semiconductor (CMOS) logic circuits at small scale are pass transistor logic circuits. An earlier point was made about the fact that pass transistor circuits are not restoring. So, when there are a lot of layers in a cascade logic circuit, it breaks down fast. An approach to this mixed-logic design architecture that is currently under investigation involves combining the alternating phases of non-restoring and restoring logic circuits. Incorporating the most advantageous aspects of both logic topologies, this mixed-logic design attains peak performance. By using this kind of combined reasoning. In order to build 4-16 decoders, the next level requires using CMOS NOR/NAND gates in conjunction with 2-4 mixed logic pre decoders. After combining two 2-4 LPI pre-decoders with a CMOS non-inverting post-decoder, a 4-16 LP decoder may be built, as shown. Combining two 2-4 HPI decoders with a CMOS non-inverting decoder resulted in a 4-16 HP decoder that is similar to the one seen below. To build a 4-16 LPI decoder, two 2-4 LP decoders and a CMOS inverting post decoder are used, while a 4-16 HPI decoder calls for two 2-4 HP decoders and a CMOS inverting decoder. Finally, there are three different topologies for 4-16 decoders: CMOS, LP, and HP. CMOS requires 104 transistors, LP requires 92, and HP requires 94.

5. COMPARISON BETWEEN EXISTING AND PROPOSED METHOD

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COMPARISION TABEL

S.No	method	AVG POWER	STATIC POWER	DYNAMIC POWER	DELAY
1.	4A	509.8E-9	721P	80.69µ	100.7E-9
2.	4B	530.8E-9	680.47P	992.41P	211.8E-12

6. CONCLUSION

The use of Mentor Graphics 16nm Technology has allowed for the validation of this project. Decoders that combine static CMOS, TGL, and DVL circuits are now available in an efficient mixed logic architecture. For the purpose of designing low power and high performance decoders, two new topologies are suggested. There are two types of decoders used in each scenario: normal and inverting 2-4 and 4-16, with and without enable input. The simulation findings show that the 2-4 and 4-16 LP LPI decoders are ideal for situations where space and power consumption are key design considerations, since they enhance power efficiency while reducing the number of transistors required. Improved power and delay performance with fewer transistors distinguishes the 2-4 and 4-16 HP, HPI decoders from conventional CMOS logic decoders in almost every scenario. The suggested mixed logic decoders are thus more efficient and run faster with fewer transistors.The suggested 12 Transistors 2X4 Decoder has a power dissipation of 2.95 Mw. The recommended strategy resulted in a 30% reduction in power use.

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